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A process for fabricating, in a planar substrate, a hermetically sealed chamber for a field-emission cell or the like, allows operating the device in a vacuum or a low pressure inert gas. The process includes methods of covering an opening (160), enclosing the vacuum or gas, and methods of including an optional quantity of gettering material. An example of a device using such a hermetically sealed chamber is a lateral-emitter field-emission device (10) having a lateral emitter (100) parallel to a substrate (20) and having a simplified anode structure (70). In one simple embodiment, a control electrode (140) is positioned in a plane above the emitter edge (110) and automatically aligned to that edge. The simplified devices are specially adapted for field emission display arrays. An overall fabrication process uses steps (S1-S18) to produce the devices and arrays. Various embodiments of the fabrication process allow the use of conductive or insulating substrates (20), allow fabrication of devices having various functions and complexity, and allow covering a trench opening (160) etched through the emitter and insulator, thus enclosing the hermetically sealed chamber.

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DESCRIPTION

Fabrication Process for Hermetically Sealed Chamber in Substrate

TECHNICAL FIELD

This invention relates in general to integrated microelectronic devices and relates more particularly to devices having a simplified construction especially adapted for use in displays and to simplified methods of fabricating such microelectronic devices, including methods for fabricating a hermetically sealed chamber in a substrate.

BACKGROUND OF THE INVENTION

Field-emission displays are considered an attractive alternative and replacement for liquid-crystal displays, because of their lower manufacturing cost and lower complexity, lower power consumption, higher brightness, and improved range of viewing angles. Microelectronic field-emission devices more generally are also attractive alternatives to semiconductor devices for many applications, being capable of high performance and being capable of fabrication from a wide range of materials with less stringent controls of material purity, but with fabrication processes and equipment similar to those used for semiconductor fabrication. A review article on the general subject of vacuum microelectronics was published in 1992: John H. Durn, "Vacuum Microelectronics - 1992," in Journal of Micromechanics and Microengineering, Vol. 2, No. 2 (June 1992). An article by Katherine Derbyshire, "Beyond AMLCDs: Field Emission Displays?" in Solid State Technology, Vol. 37 No. 11 (Nov. 1994) pages 55-65, summarized fabrication methods and principles of operation of some of the competing designs for field-emission devices and discussed some applications of field-emission devices to flat-panel displays. The theory of cold field emission of electrons from metals is discussed in many textbooks and monographs, including the monograph by R. O. Jenkins and W. G. Trodden, "Electron and Ion Emission From Solids" (Dover Publications, Inc., New York, NY, 1965), Chapter 4.

NOTATIONS AND NOMENCLATURE

The terms emitter and cathode are used interchangeably throughout this specification to mean a field-emission cathode. The term "control electrode" is used herein to denote an electrode that is analogous in function to the control grid in a vacuum-tube triode. Such electrodes have also been called "gates" in the field-emission device related art literature. Ohmic contact is used herein to denote an electrical contact that is non-rectifying. Phosphor is used in this specification to mean a material characterized by cathodoluminescence. In descriptions of phosphors, a conventional notation is used wherein the chemical formula for a host or matrix

compound is given first, followed by a colon and the formula for an activator (an impurity that activates the host crystal to luminesce), as in ZnS: Mn, where zinc sulfide is the host and manganese is the activator.

DESCRIPTION OF THE RELATED ART

5 Microelectronic devices using field emission of electrons from cold-cathode emitters have been developed for various purposes to exploit their many advantages including high-speed switching, insensitivity to temperature variations and radiation, low power consumption, etc. Most of the microelectronic field-emission devices in the related art have had emitters which point orthogonally to the substrate, generally away
10 from the substrate, but sometimes toward the substrate. Examples of this type of device are shown, for example, in U.S. Pat. No. 3,789,471 by Spindt et al., U.S. Pat. No. 4,721,885 by Brodie, U.S. Pat. No. 5,127,990 by Pribat et al., U.S. Pat. Nos. 5,141,459 and 5,203,731 by Zimmerman, and in the above-mentioned article by Derbyshire. In such structures, the anode is typically a transparent faceplate parallel to
15 the substrate and carrying a phosphor which produces the display's light output by cathodoluminescence. A few cold-cathode microelectronic devices have had field emitters oriented in a plane substantially parallel to their substrates, as for example in U.S. Pat. No. 4,728,851 by Lambe, U.S. Pat. No. 4,827,177 by Lee et al., and U.S. Pat. Nos. 5,233,263 and 5,308,439 by Cronin et al. The terminology "lateral field
20 emission" and "lateral cathode" or "lateral emitter" of the latter two patents by Cronin et al. will be adopted herein to refer to a structure in which the field emitter tip or blade edge points in a lateral direction, i.e. substantially parallel to the substrate. In such lateral cathode structures of the prior art the anode is oriented substantially orthogonally to the substrate and to the emitter (as in U.S. Pat. Nos. 5,233,263 and
25 5,308,439 by Cronin et al.), or is coplanar with the emitter (as in U.S. Pat. No. 4,827,177 by Lee et al.), or requires a transparent substrate (as in U.S. Pat. No. 4,728,851 by Lambe). Some device structures and fabrication processes using lateral cathode configurations have been found to have distinct advantages, such as extremely fine cathode edges or tips and precise control of the inter-element dimensions,
30 alignments, capacitances, and of the required bias voltages.

PROBLEMS SOLVED BY THE INVENTION

If lateral field-emission devices are used in a display cell with phosphor-coated anodes, a number of problems occur. In some of the prior art structures, the cathodoluminescence occurs only at a very narrow region at an edge of the anode facing the lateral emitter. In others the light emitted from the phosphor can be obscured by opaque electrodes or absorbed in the phosphor layer itself or in a faceplate. In some prior art structures very high anode voltages must be used. For low voltage electron field-emission device display elements (e.g. with anode potentials of less than about 10 volts with respect to the emitter), the actual electron penetration into the phosphor is on the order of 1 nanometer. Therefore, in displays using prior art lateral electron field-emission device display elements, the light emission due to cathodoluminescence occurs along the edge of the phosphor facing the emitter element. Furthermore, other electron field-emission displays such as the Spindt type (described in the patent by Spindt et al. and in the review article by H. H. Busta cited herein above) typically emit light at a phosphor surface which is opposite the phosphor surface facing the observer.

The device structure described herein has a lateral electron emitter situated a distance above the anode phosphor. When an appropriate applied field is used, the electrons spread out over the top surface of the phosphor and light is emitted over an area of the phosphor element than with other lateral electron field-emission device display elements. Hence, with this new structure, the light is emitted in direct view of the observer and is not attenuated by passing through the phosphor as is the case with prior art structures. Also, the light is generated over a larger portion of the cell area than in prior art structures. The prior art descriptions of lateral-emitter field-emission display elements do not show how to provide a bias voltage contact to the phosphor of such an anode element. The new structure described herein has a metal anode contact situated below the phosphor ("buried") and also may have means for connecting to that buried contact from the surface for applying electrical bias. In particular, the simplified structure may be fabricated within a hermetically sealed chamber in the substrate.

While the lateral-emitter type of construction has the distinct advantages described above, those lateral-emitter field-emission devices heretofore available having the most precise control of inter-element dimensions and alignment have been somewhat expensive to fabricate because of the relatively large number of materials and process steps used. Those process steps have included steps using conformal layers of sacrificial materials needed to form spacers that define some of the dimensions. The present invention eliminates some of the materials and process steps needed for fabrication, thus reducing fabrication time and cost and also providing a

simplified anode structure, while retaining the advantages of lateral cathode construction and inherently automatic alignment of the lateral cathode type of design. This simpler structure and simpler, less expensive fabrication are effective both for field-effect devices having phosphor anodes used for display elements and for field-effect devices without phosphor. Thus the present invention solves several problems existing in the prior art.

PURPOSES, OBJECTS, AND ADVANTAGES OF THE INVENTION

An important object of the invention is providing a display with improved light emission from each cell of the display. A related object is a field-emission device structure specially adapted for use in a display cell. Another related object is a field-emission display which allows light emitted from a phosphor to be aimed more directly toward the viewer of the display. Another related object is a field-emission display cell structure in which the light emission area occupies a larger portion of the cell area than in prior art devices of the lateral-emitter type. Another object of the invention is a metallization structure that allows the other features and advantages of an improved lateral-emitter field-emission display device to be realized. A particular object is an anode electrical contact structure that does not obscure any portion of a phosphor area in a display cell. A related object is an anode structure that is adapted to reflect emitted light toward the observer of the display. Another object is a display cell anode structure that provides improved performance with coulombic aging of the phosphor thereby being reduced or eliminated. Another particular object is a display cell simplified by having a control electrode configuration that may be made with a single metallization step. An overall object of the invention is an improved display which nevertheless retains all the known advantages of lateral-emitter field-emission devices, including the following: extremely fine cathode edges or tips; exact control of the cathode-to-anode distance (to reduce device operating voltage and to reduce device-to-device variability); exact control of the cathode-to-control-electrode distance (to control the control-electrode-to-cathode overlap, and thereby control the inter-electrode capacitances and more precisely control the required bias voltage); inherent alignment of the control-electrode and cathode structures; self-alignment of the anode structure to the control-electrode and cathode; and improved layout density. Another object of the invention related to retaining known advantages of lateral-emitter field-emission devices is the significant design flexibility provided by an integrated structure which reduces the number of interconnections between devices, thus reducing costs and increasing device reliability and performance. Another important object of the invention is a process using existing microelectronic fabrication techniques and apparatus for making integrated lateral-emitter field-emission display device cell

structures with economical yield and with precise control and reproducibility of device dimensions and alignments. A major object of the invention is a simplified anode structure for lateral-emitter field-emission devices. Another major object of the invention is a fabrication process which eliminates some masks otherwise needed for fabrication of a self-aligned lateral-emitter field-emission device, thus reducing fabrication time and cost.

SUMMARY OF THE INVENTION

In one aspect of the invention, a field-emission device is made with a lateral emitter substantially parallel to a substrate and with a simplified anode structure. The lateral-emitter field-emission device has a thin-film emitter cathode which has a thickness of not more than several hundred angstroms and has an emitting blade edge or tip having a small radius of curvature. The simplified anode device may also have one or more control electrodes. The anode's top surface is precisely spaced apart from the plane of the lateral emitter and receives electrons emitted by field emission from the blade edge or tip of the lateral-emitter cathode, when a suitable bias voltage is applied. The device may be configured as a diode, or as a triode, tetrode, etc. having one or more control electrodes positioned to allow control of current from the emitter to the anode by an electric field applied to the control electrode. In one embodiment, a single or more control electrodes positioned in a plane parallel to the emitter edge or tip and automatically aligned to that edge. The simplified devices are specially adapted for use in arrays, including field-emission display arrays.

In another aspect of the invention, a novel fabrication process using process steps similar to those of semiconductor integrated circuit fabrication is used to produce the novel devices and their arrays. Various embodiments of the fabrication process allow the use of conductive or insulating substrates and allow fabrication of devices having various functions and complexity. The anode is simply fabricated, without the use of prior art processes which formed a spacer made by a conformal coating. In a preferred fabrication process for the simplified anode device, the following steps are performed: an anode film is deposited; an insulator film is deposited over the anode film; an ultra-thin conductive emitter film is deposited over the insulator and patterned; a trench opening is etched through the emitter and insulator, stopping at the anode film, thus forming and automatically aligning an emitting edge of the emitter; and means are provided for applying an electrical bias to the emitter and anode, sufficient to cause field emission of electrons from the emitting edge of the emitter to the anode. The anode film may comprise a phosphor for a device specially adapted for use in a field-emission display. The fabrication process may also include steps to deposit

additional insulator films and to deposit additional conductive films for control electrodes, which are automatically aligned with the emitter blade edge or tip.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a plan view of a portion of a preferred array embodiment of field-emission devices made in accordance with the invention.

Fig. 2 shows a side elevation cross-sectional view of an embodiment of a single field-emission device made in accordance with the invention.

Fig. 3 shows a side elevation cross-sectional view of an alternate embodiment of a single field-emission device.

Figs. 4a and 4b together show a flow diagram of an embodiment of a fabrication process performed in accordance with the invention.

Figs. 5a and 5b together show a series of side elevation cross-sectional views corresponding to results of the process steps of Figs. 4a and 4b.

BRIEF DESCRIPTION OF TWO PREFERRED EMBODIMENTS

Fig. 1 shows a plan view of a portion of a preferred array embodiment of field-emission devices made in accordance with the invention. In the simple array of Fig. 1, each field-emission device shares an anode with at least one other device, and each anode is shared by two or more devices. Some of the emitters in Fig. 1 are also shared by two devices. This sharing of elements between devices is not necessary for use or operation of the invention, but it is sometimes useful in designing and fabricating arrays with higher density (in terms of the number of devices per unit area). The basic features of devices made in accordance with the invention may be clearly understood by considering the single device of Fig. 2.

Fig. 2 shows a side elevation cross-sectional view of an embodiment of a single field-emission device made in accordance with the invention. The field-emission device, denoted generally by 10, is made on a flat substrate 20. A layer of insulator 30 has a top major surface, which defines a reference plane 40 convenient for description of other elements. A layer of conductive material 50 may be used as a buried contact layer. It should be noted that conductive layer 50 may lie on the reference plane, as shown in Fig. 2, or may be made by depositing conductive layer 50 into recesses formed in insulator 30 and by planarizing the resulting surface. In the latter case the top surface of conductive layer 50 lies in reference plane 40. A layer of insulator 60 is

made on the reference plane 40, covering conductive layer 50. A conductive layer parallel to plane 40 serves as an anode 70. As will become apparent from a reading of the remainder of this specification and the appended claims, the preferred fabrication process described herein below automatically places the top surface of anode 70 below the plane of lateral emitter 100. For embodiments such as that of Fig. 2, in which some devices have independent anodes, the anodes of adjacent devices are separated and insulated from each other by regions of an insulator 80. At the left side of Fig. 2, a small portion of the anode 70 of an adjacent device is shown to the left of insulator 80; that portion is not involved in the structure or operation of the single device of the present description. An insulating layer 90 of predetermined thickness is made parallel to the substrate. An ultra-thin conductive layer which forms an emitter layer 100 is also made parallel to the substrate and patterned, thus forming a lateral emitter. A conductive contact 120 may connect emitter layer 100 to buried contact layer 50. If the device is to have a control electrode 140 above emitter 100, then two additional layers are made: a layer of insulator 130 and a conductive layer patterned to form a control electrode 140. In the fabrication process for this device (described in more detail herein below), an opening 160 is provided by employing a directional etch. That opening extends through all the layers of conductors and/or insulators above the emitting edge or tip 110 of the lateral emitter 100. The blade edge or tip 110 has a very small radius of curvature, limited by half the thickness of the ultra-thin lateral-emitter layer 100. Preferred thicknesses of lateral-emitter film 100 are less than about 300 angstroms, which limit the radius of curvature of lateral-emitter blade edge or tip to be less than about 150 angstroms. Those skilled in the art will recognize that the radius of curvature is a significant factor in producing an electric field at tip 110 sufficient to cause cold-cathode field emission at a low applied bias voltage, and that the radius of curvature may be somewhat less than half of the film thickness. Another factor significant in determining the electric field effective in causing field emission is the (predetermined) thickness of insulator film 90. The degree of film thickness control in conventional semiconductor integrated processing is sufficient to control the thickness of insulator film 90 to the desired precision. Devices made in accordance with the present invention may be operated at applied bias voltages of 10 to 50 volts or even less. In the preferred embodiment of Fig. 2, anode 70 extends at least partially under lateral emitter 100. That is, anode 70 extends beyond the vertical plane through emitting edge 110 defined by the side wall of opening 160.

It should be noted that conductive connections to the various electrodes of the device may be made in a conventional manner, and are therefore not shown in the

drawings. These conductive connections may be made, for example, by vertical studs that lie outside the plane of the side elevation cross-section view of Fig. 2. For example, a conductive stud may extend from emitter 100 and/or buried contact layer 50 to a surface conductive pad to which the emitter bias voltage may be applied. A similar conductive connection, electrically isolated from the emitter connection, may be made to anode 70, for application of the anode bias voltage. Similarly, conductive connections are needed to apply control signals to control electrode(s) 140 if the device is a triode or tetrode, etc. having such control electrodes. The arrangement just described may also be reversed, in the sense that the emitter connection may be made directly to a surface pad, and buried contact layer 50 may be used for anode contacts. Of course, for field emission of electrons to occur, the polarity of applied bias voltages must be such that the anode is positive with respect to the emitter. Various devices made on the same substrate need not have identical physical arrangements of conductive connections. Some devices may have buried anode contacts, while other devices on the same substrate may have buried emitter contacts. Such arrangements are not intended to limit the scope of the invention. For example, a device is to be connected to an anode of another device. With such arrangements, dissimilar connections lying in the same plane and not intended to be connected may be connected to the same anode or emitter. The scope of the invention is not limited by the particular physical arrangements of connections shown in the drawings.

Fig. 3 shows a side elevation cross-sectional view of an alternate embodiment of a single field-emission device made in accordance with the invention. The lateral-emitter field-emission device of Fig. 3 is a diode device, without a control electrode. The anode of the device shown in Fig. 3, denoted generally by 70, includes a phosphor layer 75, which is a part of anode 70. If the anode phosphor is conductive, the entire anode 70 may consist of phosphor. The anode 70 of Fig. 3 is shown with a separately identified phosphor film 75 to illustrate an alternative embodiment. The device of Fig. 3 also differs from Fig. 2 in that anode 70 does not extend beneath emitting blade edge or tip 110 of lateral emitter 100. Another way of describing the alternative structure shown in Fig. 3 is that opening 160, the sidewall of which defines the vertical plane containing emitting edge 110 of lateral emitter 100, extends beyond the horizontal extent of anode 70. However the vertical extent of opening 160 is still determined by the fact that opening 160 extends vertically only to the top surface of anode 70 (which in this embodiment is the top surface of phosphor film 75). The minimum vertical extent of opening 160 in the device of Fig. 3 is the sum of the predetermined thickness of insulator layer 90 and the predetermined thickness of lateral emitter 100. The field-emission device may be made with a plurality of anodes 70 (not shown in the drawings). A useful example of such a structure has three anodes per emitter, with a

different phosphor color of each anode. A particularly useful combination is a three-anode device with red, green, and blue phosphors for an RGB display.

Operable and preferred materials for the various structural elements of the lateral-emitter field-effect device with simplified anode are described herein below in connection with an exposition of a novel and preferred fabrication process.

A novel fabrication process using process steps similar to those used in semiconductor integrated circuit fabrication may be used to produce the devices and their arrays in accordance with the invention. Various embodiments of the fabrication process allow the use of conductive or insulating substrates and allow fabrication of devices having various functions and complexity. A notable feature of all the fabrication process embodiments described herein is that the anode is simply formed without the use of a spacer employed in some prior art processes. (In those prior art processes, a spacer was formed by a sacrificial conformal coating.)

Figs. 4a and 4b together with a flow diagram of the fabrication of the diode device are shown in Figs. 5a and 5b. The fabrication process performed in accordance with the invention. Figs. 5a and 5b together show a series of side elevation cross-sectional views of the device at various stages of the process. The process steps shown in Figs. 4a and 4b are further illustrated by the corresponding results of Figs. 5a and 5b. A simple overall process outline for fabrication of a diode device is described first, followed by a description of the detailed process which is depicted in Figs. 4a and 4b and which is further illustrated by the corresponding results of Figs. 5a and 5b. Table I lists the process steps shown in Figs. 4a and 4b.

In a simple fabrication process for a diode field-emission device with simplified anode, the following steps are performed: an anode film 70 is deposited (S7); an insulator film 90 is deposited (S8) over the anode film; an ultra-thin conductive emitter film 100 is deposited (S12) over the insulator and patterned; a trench opening 160 is etched (S15) through the emitter and insulator, stopping at the anode film, thus forming and automatically aligning an emitting edge 110 of the emitter; and means are provided (S18) for applying an electrical bias to the emitter and anode, sufficient to cause field emission of electrons from the emitting edge 110 of the emitter 100 to the anode 70. The anode film 70 deposited in step S7 may comprise a phosphor film 75 for a device specially adapted for use in a field-emission display. The phosphor may be any cathodoluminescent material, and may be selected on the basis of its conductivity and/or the color of its luminescence.

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|-----------|------------|--|
| | S1 | Provide substrate |
| | S2 | Deposit insulating layer |
| 5 | S3 | Pattern and etch recesses |
| | S4 | Deposit conductive material in recesses to form buried contact layer |
| | S5 | Planarize |
| | S6 | Deposit insulating layer |
| | S7 | Deposit conductive layer to a predetermined thickness |
| 10 | S8 | Deposit insulating layer to a predetermined thickness |
| | S9 | Deposit conductive layer to form control electrode layer |
| | S10 | Deposit insulating layer to a predetermined thickness |
| | S11 | Provide conductive contacts to buried contact layer |
| | S12 | Deposit and pattern ultra-thin emitter layer |
| 15 | S13 | Deposit insulating layer to a predetermined thickness |
| | S14 | Deposit and pattern control electrode layer if any |
| | S15 | Provide opening down to anode top surface |
| | S16 | Open contact holes to emitter, control electrode (if any) and anode contact |
| 20 | S17 | Deposit metal contacts |
| | S18 | Provide means for applying suitable bias and signal voltage(s) |

Table I. List of fabrication process steps shown in Figs. 4a and 4b.

A fabrication process for a triode, tetrode, etc. device may also include steps to deposit additional insulator films 130 and to deposit additional conductive films 140 for control electrodes, which have a control electrode edge 150 automatically aligned with the emitter blade edge or tip 110. In the following detailed process description, these additional steps are included as "optional" steps, to be performed only if control electrodes are to be included in a particular device structure. It will be apparent to one skilled in the art that the detailed process of Figs. 4a and 4b, illustrated by the results of Figs. 5a and 5b, may be modified to fabricate simpler devices by omitting particular process steps as appropriate. Other variations in technique and in the order of process steps will also be apparent to one skilled in the art.

A detailed description of a preferred process for fabricating the field-emission devices now proceeds, with reference to Figs. 4a, 4b, 5a, and 5b.

To fabricate a triode device with one or two control electrodes, the process illustrated in Figs. 4a, 4b, 5a and 5b is performed. A substrate 20 is provided (step S1), which may be a silicon wafer. An insulating layer 30 is deposited (step S2) on the substrate. This may be done, for example, by growing a film of silicon oxide on the substrate, or by depositing a film of silicon oxide on the substrate. A pattern of recesses is defined and etched (step S3) into the surface of the insulating layer. In step S4, metal is deposited in the recesses to form a buried contact layer 50, which is then planarized (step S5). While this is described here as a metal deposition, the conductive material deposited in step S4 may be a metal such as aluminum, tungsten, titanium, etc., or may be a transparent conductor such as tin oxide, indium tin oxide etc. (For applications using a common emitter for all devices made on a substrate, the substrate may be conductive and perform the function of a buried emitter contact. For such applications, steps S2, S3, S4, and S5 may be omitted, although a step similar to step S2 may be required to insulate a control electrode if any from the substrate.) An insulating layer 60 is deposited (step S6). This may be a chemical vapor deposition of silicon oxide to a thickness of about 0.1 to 2 micrometers, for example.

A conductive layer is deposited (step S7) to a predetermined thickness and patterned to form an anode layer 70. If anode 70 is not required to be cathodoluminescent in order to function as a light source, then the conductive anode layer 70 deposited in step S7 may be a metal film or another conductive film such as indium oxide or indium tin oxide (ITO). If the device is to be used in a light-emitting application, such as a display, the conductive layer may be a conductive phosphor 75 or may be a composite layer comprising a conductive material with a thin film of

phosphor 75 on its top surface. Suitable phosphors include zinc oxide (ZnO), zinc sulfide (ZnS) and many other compounds. Some other suitable phosphors are ZnO:Zn; $\text{SnO}_2\text{:Eu}$; $\text{ZnGa}_2\text{O}_4\text{:Mn}$; $\text{La}_2\text{O}_2\text{S:Tb}$; $\text{Y}_2\text{O}_2\text{S:Eu}$; LaOBr:Tb ; $\text{ZnS:Zn+In}_2\text{O}_3$; $\text{ZnS:Cu,Al+In}_2\text{O}_3$; $(\text{ZnCdS:Ag+In}_2\text{O}_3)$; and $\text{ZnS:Mn+In}_2\text{O}_3$. Still other suitable phosphor materials are described, for example, in the chapter by Takashi Hase et al. "Phosphor Materials for Cathode Ray Tubes" in "Advances in Electronics and Electron Physics" Vol. 79 (Academic Press, San Diego, CA, 1990), pages 271-373, which reference also uses the conventional phosphor notation used here. If the application requires anode layer 70 to be patterned, that patterning may be done by subprocesses that are conventional in semiconductor fabrication practice, using lithography and etching to pattern the layer. In particular, anode layer 70 may be formed and patterned by a process analogous to steps S3, S4, and S5.

In the next step (S8), an insulating layer 90 is deposited to a precisely predetermined thickness. This predetermined thickness of insulating layer 90 is quite important in determining the emitter-to-anode closest distance, and thus in determining the electric field produced by a given applied bias voltage. Step S8 may involve chemical vapor deposition of silicon oxide to a predetermined thickness. In the case of

Steps S8 and S9 are performed, a control electrode layer 140 is deposited below the emitter layer 100. (Such a control electrode layer is shown in Fig. 5a, but then omitted from Fig. 5b to illustrate the option without a lower control electrode layer.) If needed, a conductive control electrode layer 140 is deposited and patterned in step S9. In step S10 an insulating layer 130 of a predetermined thickness is deposited over conductive control electrode layer 140 to insulate it and to provide a flat insulating surface parallel to the substrate for the next step. Whether or not steps S9 and S10 are performed, a planar insulating surface is provided.

This description of a fabrication process continues with reference to Fig. 4b and Fig. 5b, respectively showing the remaining fabrication steps and the corresponding side cross sectional views of the device. In step S11, conductive contacts 120 are provided to the buried contact layer 50, by opening suitable contact holes and depositing conductive material in them (forming "studs") to make ohmic contact with buried contact layer 50. In step S12, an ultra-thin emitter layer 100 is deposited and patterned. Preferred materials for conductive lateral-emitter layer 100 are titanium, tungsten, tantalum, molybdenum, or their alloys such as titanium-tungsten alloy. However, many other conductors may be used, such as aluminum, gold, silver, copper, copper-doped aluminum, platinum, palladium, polycrystalline silicon, etc. or transparent thin-film conductors such as tin oxide or indium tin oxide (ITO). It is very

desirable to use a material with a low work function for electron emission. In this respect, preferred materials have work functions less than three electron volts, and even more preferred materials have work functions of less than one electron volt. The deposition in step S12 is controlled to form a film preferably of about 100 - 300
 5 ångstroms thickness in order to have an emitter blade edge or tip 110 in the final structure that has a radius of curvature preferably less than 150 ångstroms and more preferably less than 50 ångstroms. To fabricate the preferred embodiment of Fig. 2, patterning of lateral emitter 100 is done so that lateral emitter 100 extends over at least a portion of anode 70. An insulator 130 is deposited (step S13) over the emitter layer.
 10 Again this may be a chemical vapor deposition of silicon oxide to a thickness of about 0.1 to 2 micrometers, for example. If there are to be two control electrodes and if symmetry with respect to the plane of emitter layer 100 is desired, then this insulator layer 130 should be made the same thickness as the insulator layer 130 deposited in step S10. If a control electrode 140 is to be incorporated, a conductive material is
 15 deposited and patterned (step S14) to form the upper control electrode layer 140. (The lower control electrode 140 will be deposited in a subsequent step, as in the case of the buried control layer 50.) It should be mentioned that the conductive films deposited and patterned in steps S14, S9 (if provided), and S14 are deposited and patterned in a similar manner to that of the emitter layer 100.

In step S15, an opening is provided through all the layers lying over anode 70, down to the top surface of anode layer 70. This opening is patterned to intersect at least some portions of emitter layer 50 (and of control electrode layers 140 if any), to
 25 define emitting edge 110 of emitter layer 100 (and to define edge 150 of control electrode layer 140 if any). This step is performed by using conventional directional etching processes such as reactive ion etching sometimes called "trench etching" in the semiconductor fabrication literature. To fabricate the preferred embodiment of Fig. 2, step S15 is performed while leaving at least a portion of insulator 90 remaining and covering at least a portion of anode 70.

In step S16, contact holes are opened to emitter, control electrode, and anode if needed. Metal contacts are deposited where needed in step S17. Alternatively, this part of the process (steps S16 and S17) may be performed after step S13 or S14 but
 30 before S15. In that case, the sequence of process steps would be as follows: S13, S14 (if used), S16, S17, and then S15. It should be noted that for some display applications (such as so-called "heads-up" displays), it is desirable to form the device structure using substantially transparent materials for all the films. With the operable and preferred thicknesses of the films in the present invention, such transparent films may be made if desired.

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getter materials known in the art of vacuum tube construction. This process for retaining vacuum or gas atmospheres is not illustrated in Figs. 4a, 4b, 5a, and 5b.

It will be appreciated by those skilled in the art that integrated arrays of field-emission devices, such as the array of Fig. 1, may be made by simultaneously
 5 performing each step of the fabrication process described herein for a multiplicity of field-emission devices on the same substrate, while providing various interconnections among them. An integrated array of field-emission devices made in accordance with the present invention has each device made as described herein, and the devices are
 10 arranged as cells containing at least one emitter and at least one anode per cell. The cells are arranged along rows and columns, with the anodes interconnected along the columns for example, and the emitters interconnected along the rows.

INDUSTRIAL APPLICABILITY

There are many diverse uses for the hermetically sealed chamber, device structure, and fabrication processes of the invention, especially in making flat-panel displays for displaying images and for displaying character or graphic information. Displays made in accordance with the present invention are expected to have higher brightness, higher contrast, and improved range of viewing angles. Displays made in accordance with the present invention are also expected to be used in new applications such as
 15 displays for virtual reality systems. In embodiments using substantially transparent substrates and films, displays incorporating the structures of the present invention are especially useful for augmented-reality displays.

Other embodiments of the invention will be apparent to those skilled in the art from a consideration of this specification or from practice of the invention disclosed
 25 herein. For example the order of process steps may be varied to some extent for various purposes; improved lithographic patterning, deposition, etching, or other process techniques may be used; functionally equivalent materials may be substituted for the particular materials used in the embodiments described herein; preferred
 30 dimensions may be varied; and other modifications may be made to adapt the device to various usages and conditions. The hermetically sealed chamber may be used to enclose and protect various microelectronic devices other than field-emission devices. It is intended that the specification and examples be considered as exemplary only, with the true scope and spirit of the invention being defined by the following claims.

35 Having described my invention, I claim:

CLAIMS

1. A process for forming an evacuated chamber in a substrate having an upper surface, comprising the steps of:
 - (a) providing a first opening in said upper surface of the substrate, said opening having a first predetermined depth and a predetermined volume, to form a main cavity;
 - (b) providing a second opening, communicating with said first opening provided in step (a), said second opening having a second predetermined depth;
 - (c) temporarily filling both said first and second openings with a sacrificial first material;
 - (d) planarizing said sacrificial first material to form a planar surface;
 - (e) disposing a second material over said upper surface of the substrate and said planar surface to form a chamber ceiling;
 - (f) providing a third opening in said chamber ceiling only, over said second opening;
 - (g) removing any atmosphere surrounding and within said chamber formed in step (e) to evacuate said chamber;
 - (h) introducing a gettering material into said third opening; and
 - (i) then immediately introducing a third material into said second and third openings, while plugging said third opening and while sealing said third material to said second material, thereby enclosing said evacuated chamber.
2. A process as recited in claim 1, wherein said first-opening-providing step (a) is performed by directionally etching said upper surface of the substrate.
3. A process as recited in claim 1, wherein said first-opening-providing step (a) is performed by reactive ion etching of said upper surface of the substrate.
4. A process as recited in claim 1, wherein said second-opening-providing step (b) is performed by controlling said second predetermined depth to be less than said first predetermined depth of said first opening.
5. A process as recited in claim 1, wherein said temporarily-filling step (c) is performed by depositing an organic material as said sacrificial first material.

6. A process as recited in claim 1, wherein said temporarily-filling step (c) is performed by depositing parylene as said sacrificial first material.
7. A process as recited in claim 1, wherein said second-material-disposing step (e) is performed by disposing an inorganic material.
- 5 8. A process as recited in claim 1, wherein said sacrificial-first-material-removing step (g) is performed by isotropically etching said sacrificial first material.
9. A process as recited in claim 1, wherein said sacrificial-first-material-removing step (g) is performed by etching said sacrificial first material with oxygen plasma.
- 10 10. A process as recited in claim 1, wherein said third-material-introducing step (j) is performed by sputter-depositing said third material.
11. A process as recited in claim 1, wherein said third-material-introducing step (j) is performed by sputter-depositing an inorganic material.
12. A process as recited in claim 1, wherein said gettering-material-introducing step (i) comprises introducing a material selected from the list consisting of Ca, Ba, Ti, alloys of Th, and compounds, mixtures, and solutions thereof, and oxygen and materials suitable for gettering gases containing sulfur.
14. A process as recited in claim 1, wherein said gettering-material-introducing step (i) comprises introducing a material selected from the list consisting of Ca, Ba, Ti, alloys of Th, and compounds, mixtures, and solutions thereof.
- 20 15. A process for forming a gas-filled chamber in a substrate having an upper surface, comprising the steps of:
 - 25 (a) providing a first opening in said upper surface of the substrate, said opening having a first predetermined depth and a predetermined volume, to form a main cavity;
 - (b) providing a second opening, communicating with said first opening provided in step (a), said second opening having a second predetermined depth;
 - 30 (c) temporarily filling both said first and second openings with a sacrificial first material;
 - (d) planarizing said sacrificial first material to form a planar surface;
 - (e) disposing a second material over said upper surface of the substrate and said planar surface to form a chamber ceiling;

- (f) providing a third opening in said chamber ceiling only over said second opening;
- (g) removing said sacrificial first material from beneath said chamber ceiling through said third opening to form a chamber;
- 5 (h) removing any atmosphere surrounding and within said chamber formed in step (g) to evacuate said chamber;
- (i) introducing said gas at a desired pressure into the chamber;
- (j) introducing a gettering material into said third opening, and
- (k) then immediately introducing a third material into said second and third
- 10 openings, while plugging said third opening and while sealing said third material to said second material, thereby enclosing said gas-filled chamber.
16. A process as recited in claim 15, wherein said gas-introducing step (i) is performed by introducing an inert gas.
- A process as recited in claim 15, wherein said second-opening-providing step (b) is performed by directionally etching said upper surface of the substrate.
- A process as recited in claim 15, wherein said second-opening-providing step (b) is performed by reactive ion etching of said upper surface of the substrate.
19. A process as recited in claim 15, wherein said second-opening-providing step (b) is performed by controlling said second predetermined depth to be less than said
- 20 first predetermined depth of said first opening.
20. A process as recited in claim 15, wherein said temporarily-filling step (c) is performed by depositing an organic material as said sacrificial first material.
21. A process as recited in claim 15, wherein said temporarily-filling step (c) is performed by depositing parylene as said sacrificial first material.
- 25 22. A process as recited in claim 15, wherein said second-material-disposing step (e) is performed by disposing an inorganic material.
23. A process as recited in claim 15, wherein said sacrificial-first-material-removing step (g) is performed by isotropically etching said sacrificial first material.
24. A process as recited in claim 15, wherein said sacrificial-first-material-removing
- 30 step (g) is performed by etching said sacrificial first material with oxygen plasma.
25. A process as recited in claim 15, wherein said third-material-introducing step (j) is performed by sputter-depositing said third material.

26. A process as recited in claim 15, wherein said third-material-introducing step (j) is performed by sputter-depositing an inorganic material.
27. A process as recited in claim 15, wherein said gettering-material-introducing step (i) comprises introducing an inorganic gettering material into at least said third opening.
28. A process as recited in claim 15, wherein said gettering-material-introducing step (i) comprises introducing a material selected from materials suitable for gettering oxygen and materials suitable for gettering gases containing sulfur.
29. A process as recited in claim 15, wherein said gettering-material-introducing step (i) comprises introducing a material selected from the list consisting of Ca, Ba, Ti, alloys of Th, and compounds, mixtures, and solutions thereof.

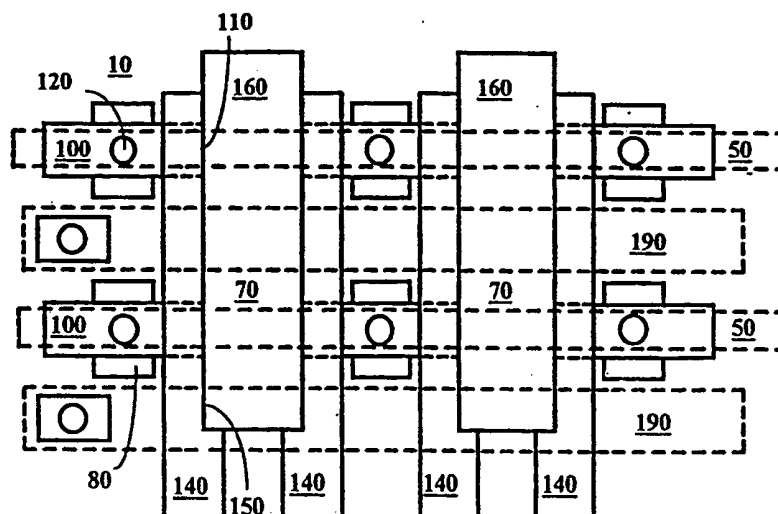


Fig. 1

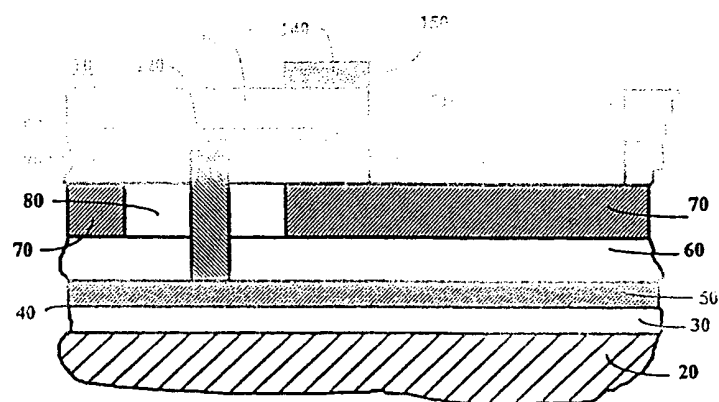


Fig. 2

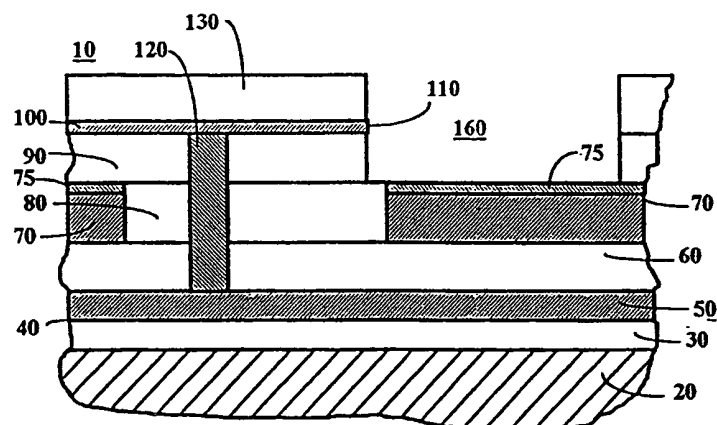


Fig. 3

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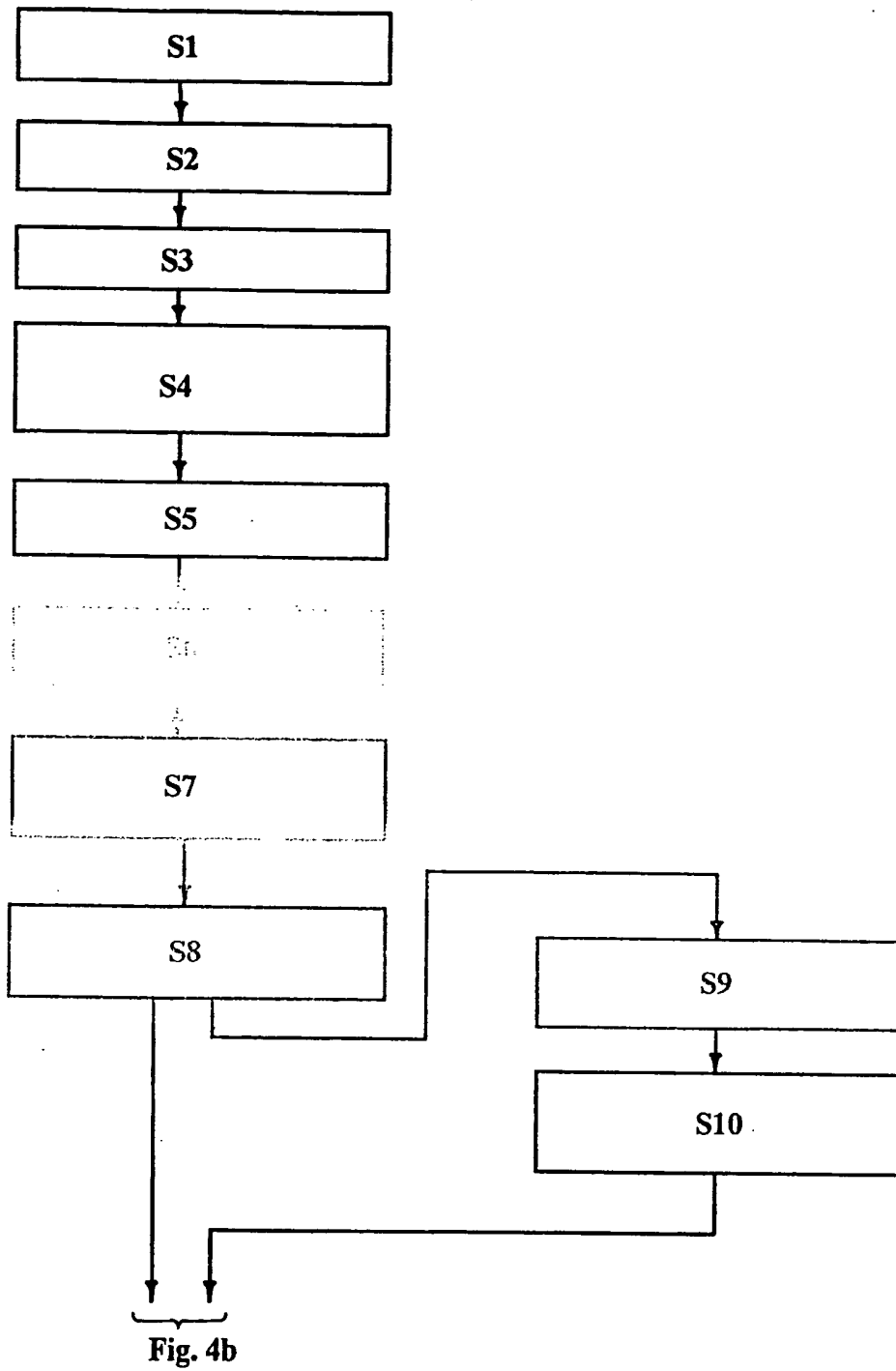


Fig. 4a

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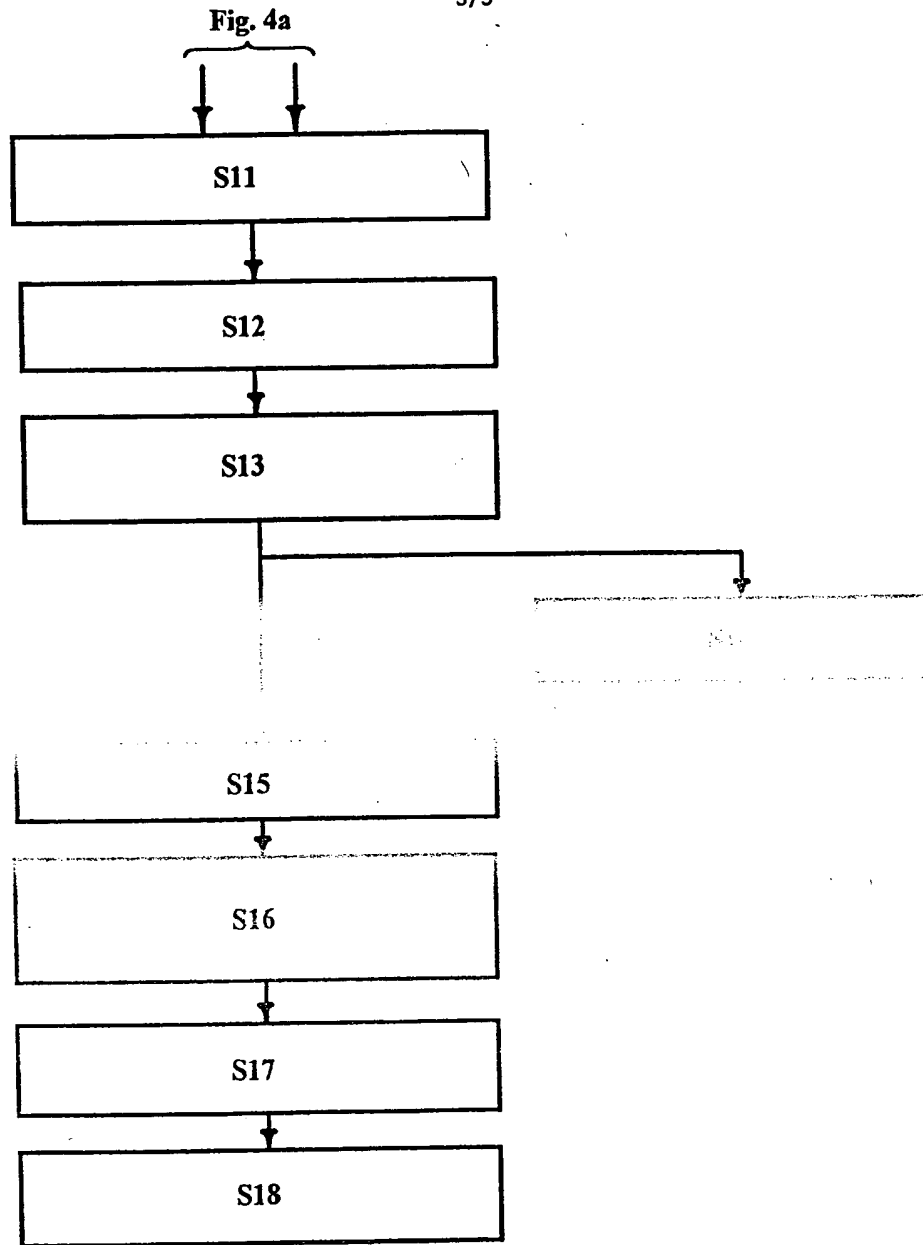


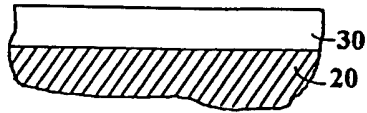
Fig. 4b

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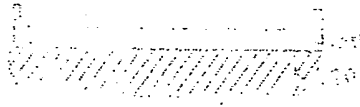
S1



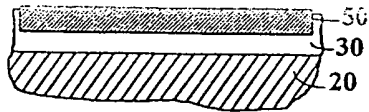
S2



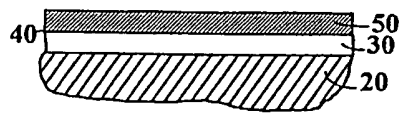
S3



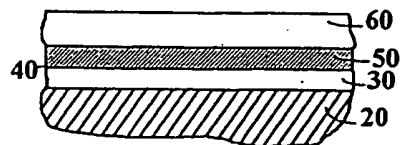
S4



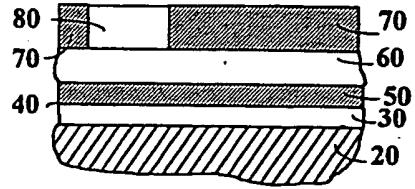
S5



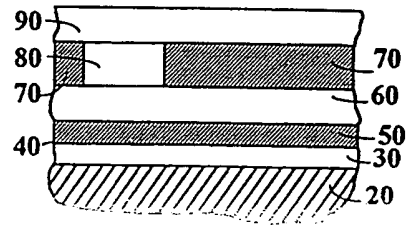
S6



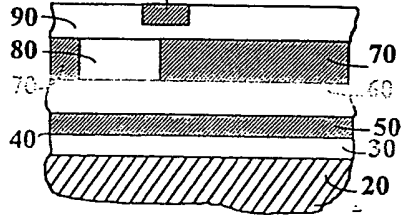
S7



S8



S9



S10

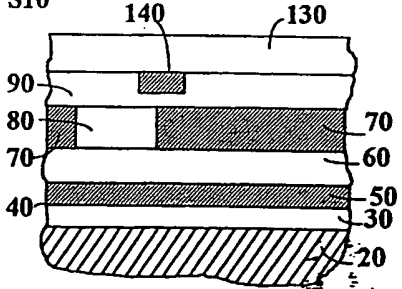
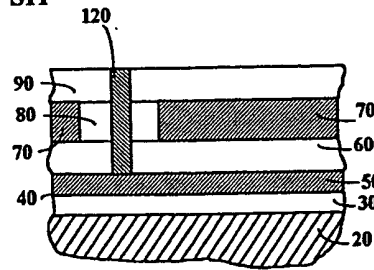


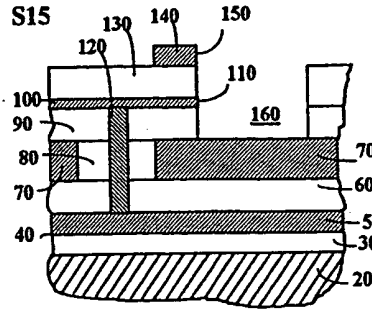
Fig. 5a

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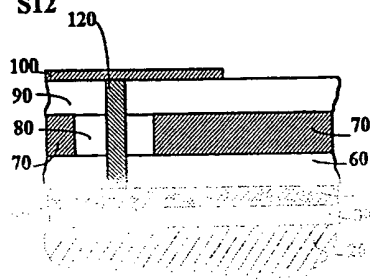
S11



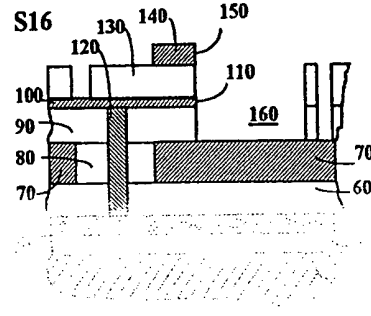
S15



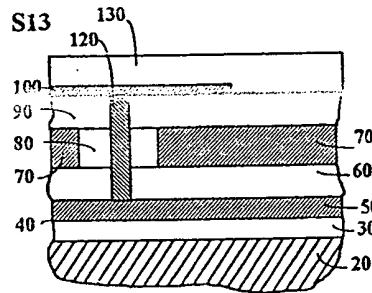
S12



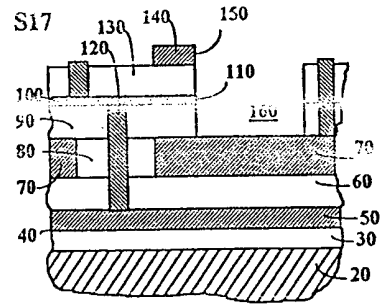
S16



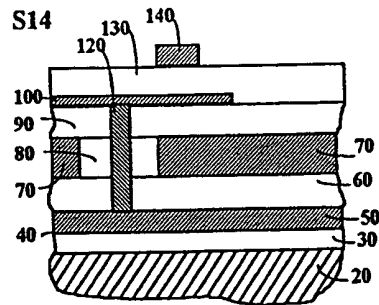
S13



S17



S14



S18

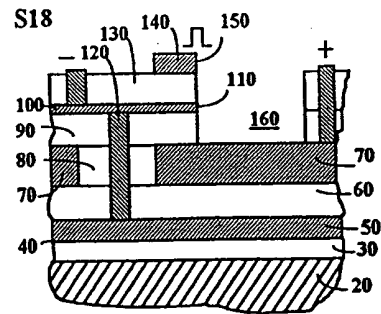


Fig. 5b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/08237

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01J 9/40

US CL :445/41,43

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 445/41,43;313/309,336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONEElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,855,636 (BUSTA ET AL) 08 AUGUST 1989, JOURNAL OF MICROWAVE TECHNOLOGY AND APPLICATIONS, 3(2), 1989, 1-10	

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

Special categories of cited documents:	
A document defining the general state of the art which is not considered to be of particular relevance	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
E earlier document published on or after the international filing date	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	*A* document member of the same patent family

Date of the actual completion of the international search

24 JULY 1996

Date of mailing of the international search report

15 AUG 1996

Name and mailing address of the ISA/US
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